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DAMAGE PROFILES IN SILICON AND THEIR
IMPACT ON DEVICE RELIABILITY

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Technical Report Number 1
October 15, 1976 - March 30, 1977

Contract No. N00173-76-C-0303
Effective Date of Contract: 10/1/76
Contract Expiration Date: 4/1/78

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Advanced Research Projects Agency
ARPA Order No. 3231, Program Code No. 6D10
Form approved budget bureau No.: 22-R0293

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AD A 053538

AD No. _____
DDC FILE COPY

Unclassified

Security Classification

DOCUMENT CONTROL DATA - R&D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY (Corporate author)

International Business Machines Corporation
System Products Division, East Fishkill
Hopewell Junction, N. Y. 12533

2a. REPORT SECURITY CLASSIFICATION

Unclassified

2b. GROUP

**DAMAGE PROFILES IN SILICON
AND THEIR IMPACT ON DEVICE RELIABILITY.**

4. DESCRIPTIVE NOTES (Type of report and inclusive dates)

Scientific 15 October 1976 to 31 March 1977

5. AUTHOR(S) (First name, middle initial, last name)

G. H. Schwuttke

Technical rept. no. 1. 15 Oct 76-31
Mar 77

6. REPORT DATE

March 1977

7a. TOTAL NO. OF PAGES

14

7b. NO. OF PAGES

23

8. CONTRACT OR GRANT NO.

DD 173-76-C-1313, ARPA Order-
3231

9. ORIGINATOR'S REPORT NUMBER(S)

TR-22,219

c. DOD ELEMENT

d. DOD SUBELEMENT

9b. OTHER REPORT NO(S) (Any other numbers that may be assigned this report)

NRL ? 535441

10. DISTRIBUTION STATEMENT

57 p.

APPROVED FOR PUBLIC RELEASE
DISTRIBUTION UNLIMITED

Mar 77

11. ABSTRACT

TEN TO THE 13TH POWER

TEN TO THE 15TH POWER
50 cm

12. SPONSORING MILITARY ACTIVITY

Advanced Research Projects Agency

13. ABSTRACT

N-type Si was implanted with 200 keV Cs⁴⁰ with doses ranging from 10^{13} to 10^{15} ions/cm². After nitrogen anneal MOS capacitors were formed by thermal oxidation and Al deposition. Transmission electron microscopy was used to study the residual ion damage. A high density of vacancy clusters of 10-40 Å is observed. In addition circular stacking faults are found in the region of the Cs profile peak. Through MOS capacitance measurements a reduction of minority carrier lifetime by a factor of 10^5 was found. This is caused by the Cs distribution in the Si which is stable at high temperature treatments as confirmed by SIMS measurements.

401 914

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Unclassified

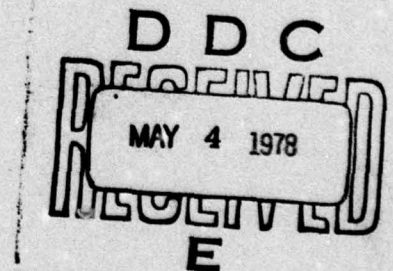
Security Classification

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	HOLE	WT	ROLE	WT
Silicon Ion implantation Defects Minority carrier lifetime						

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NTS	White Section	<input checked="" type="checkbox"/>
DSG	Buff Section	<input type="checkbox"/>
UNANNOUNCED		<input type="checkbox"/>
JUSTIFICATION		
BY		
DISTRIBUTION/AVAILABILITY CODES		
Dist.	AVAIL. and/or SPECIAL	
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Introduction

This contract is a continuation of Contract No. DAHC 15-72-C-0274 entitled "Damage Profiles In Silicon and their Impact on Device Reliability". Results of the previous contract are published in Technical Reports numbered 1 - 7. The Tables of Contents of these reports are given in the appendix.

Research to be performed under the new contract which started October 15, 1976 is outlined in the Research Plan. The work under the new contract is essentially a continuation of the original work (silicon) and also an application of this work to other materials (damage gettering in GaAs).

The following Technical Report No. 1 summarizes work that was started under the preceding contract. It is self-contained and therefore published as a separate technical report. The other work performed during the time period October, 1976 to March, 1977 relates to equipment design and building [Impact Sound Stressing (ISS)] and to damage studies in GaAs after ISS. This work is being reported separately in quarterly reports and will be summarized in the forthcoming Technical Report No. 2.

RESEARCH PROGRAM PLAN

1. Study point defects in silicon and GaAs crystals, their generation and reactions during wafer processing and their interactions with damage profiles introduced by:
 - a. Impact Sound Stressing
 - b. Ion Implantation
 - c. Diffusion
2. Produce damage profiles in silicon wafers through ion implantation techniques and study their influence on minority carrier lifetime before and after annealing.
3. Determine the influence of studies listed under (1) and (2) for Czochralski and Float Zone silicon crystals.
4. Study epitaxial layer perfection of silicon deposited on ion implanted silicon surfaces in the presence and/or absence of Impact Sound Stressed wafer backsides.
5. Study minority carrier lifetime in epitaxial layers produced as listed under (4).

6. Use advanced modern analytical characterization techniques for the studies listed under (1) to (5) such as Transmission Electron Microscopy, Scanning Electron Microscopy, X-ray Topography, Precision Lattice Parameter Measurements and Lifetime Measurements.
7. Develop new characterization techniques as needed.
8. Correlate damage measurements with electrical measurements whenever possible (relate damage profile to junction quality).

MINORITY CARRIER LIFETIME AND DEFECT STRUCTURE
IN SILICON AFTER CESIUM IMPLANTATION*

by

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ABSTRACT

It is shown that the minority carrier lifetime τ in silicon can be reduced effectively by doping with cesium. A lifetime value of 2.2×10^{-10} seconds can be achieved by implantation of $10^{13} \text{Cs}^+ / \text{cm}^2$ at 200 keV and subsequent anneal in nitrogen followed by an oxidation of 47 minutes at 1000°C . The reduction of τ in silicon is caused by the cesium distribution which is stable at this temperature. In comparison to gold the efficiency of the cesium recombination center is about 6%. Due to its low diffusion rate at high temperature cesium is proposed as a useful alternative for device applications which require gold as a dopant.

*Sponsored under ARPA Contract No. 00173-76-60303
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MINORITY CARRIER LIFETIME AND DEFECT STRUCTURE
IN SILICON AFTER CESIUM IMPLANTATION

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G. Sixt, H. Kappert and G. H. Schwuttke

INTRODUCTION

In an indirect bandgap semiconductor such as silicon, the recombination of excess minority carriers is known to occur through recombination centers which result from chemical impurities and/or crystal imperfections. This effect has practical merit for device application whenever minority carrier lifetime must be limited, such as in high speed switching devices.

Gold has the ability to provide recombination centers in silicon and is widely used in semiconductor devices to control the base minority carrier lifetime, and thus the device switching speed¹⁾.

Gold doping of semiconductor devices requires a high temperature diffusion process. The gold is normally deposited as a layer on one face of the wafer involved before diffusion. Due to the high diffusion rate of gold in silicon, this processing step must be the last one of all high temperature steps to be performed.

In spite of the importance of lifetime control in silicon for certain device applications, no alternative is available for gold doping. This paper describes the use of cesium as a dopant in silicon to achieve controlled reduction of minority carrier lifetime. Cesium has a donor level at midgap ²⁾ and has the advantage of being a slow diffuser in silicon ³⁾.

In this study, first cesium is introduced into silicon through high energy ion implantation. Thus, a controlled amount of dopant is introduced selectively at room temperature in certain wafer areas. Subsequently, ion damage in the silicon is reduced through high temperature annealing. Finally, the residual damage structure in silicon, the cesium distribution in the silicon-silicondioxide double layer, the cesium dopant concentration in silicon, and the minority carrier lifetime changes in silicon due to Cs⁺ implantation are determined through transmission electron microscopy (TEM), secondary ion mass spectrometry (SIMS), and MOS C-t measurements⁴⁾.

EXPERIMENTAL

Sample Preparation:

Czochralski-grown n-type silicon wafers of 1.2-2 Ω cm, resistivity, (100) orientation, and 2.25 inch diameter are chemically cleaned. Selected areas of the wafers are implanted with cesium ions. The implanted area is a square in the center of the wafer of about 2.7 cm sidelength. Samples designated A, B, and C are implanted, respective-

ly, with 10^{13} , 10^{14} , and 10^{15} cesium ions per square centimeter at acceleration voltages of 200 keV. After implantation the wafers are chemically cleaned and annealed in nitrogen at 1000°C for 30 minutes. Subsequently, the wafers are oxidized in the same furnace tube. The oxide layer is grown at 1000°C in dry oxygen for 10 minutes, in wet oxygen plus 2% HCl for seven minutes, and post annealed in nitrogen for 30 minutes at the same temperature.

After removal of the oxide layer on the backside of the wafers MOS capacitors are formed on the implanted and on the unimplanted parts of the wafer. Aluminum dots of 0.5 mm diameter are evaporated on the front side and aluminum metal contacts are made to the backside. A final sintering step for good ohmic contact is performed in forming gas at 400°C for 30 minutes.

The thickness of the oxide layer is determined by ellipsometer measurements.

For TEM investigations specimens of 3 mm diameter are cut ultrasonically from the implanted and unimplanted parts of the wafers. Aluminum dots and oxide layers are removed by etching in hot H_3PO_4 and HF, respectively. Subsequently, the specimens are thinned to a thickness of about 1000\AA by a standard jet-etch technique.

For SIMS measurements, square specimens of $9\text{ mm} \times 9\text{ mm}$ are cut from the implanted parts of the wafers with a diamond saw. Only the aluminum dots located on the oxide are chemically removed.

Electrical Measurements:

The minority carrier lifetime in the silicon is determined from the transient response of the MOS capacitors ⁴⁾. To avoid surface-state charging effects, the MOS capacitors are initially biased into heavy inversion. Subsequently, a depleting negative voltage step is applied to the MOS capacitors. The relaxation of the MOS capacitance with time is monitored. For transient response times of 1 msec to 1 sec an oscilloscope is used, while for times longer than 1 sec the capacitance versus time $C(t)$ curve is plotted on a X-t recorder. The measurement setup used and the computer program for lifetime data as obtained from the $C(t)$ curves are described in reference⁴⁾.

High frequency capacitance-voltage curves are measured at 1 MHz. From these curves flatband voltages V_{FB} and doping densities N_D are determined using the computer calculations of Goetzberger⁵⁾.

SIMS and TEM Measurements:

The apparatus used for the SIMS studies of the SiO_2 -Si layers is referred to as Ion-Beam Surface Mass Analyzer (ISMA) manufactured by Commonwealth Scientific Corporation. Primary argon ions with energies of 4.5 kV are directed onto the surface of the specimens at an angle of incidence of 45 degrees. Sputtered secondary ions are collected by a four-lens ion optic and analyzed in a UTI quadrupole mass analyzer. The argon pressure in the vacuum chamber is 3×10^{-6} torr at a residual gas pressure of $2 - 3 \times 10^{-7}$ torr.

For the TEM measurements a Philips EM 301 G and a JEOL 100 C electron microscope are used, operated at a voltage of 100 kV. Both microscopes are equipped with a 60 degree double tilt goniometer stage for tilt experiments. Established contrast theories are used to analyze and identify residual lattice defects⁶⁻¹⁰).

RESULTS

The effect of cesium implantation on the electrical properties of n-type silicon is shown in Figures 1a and 1b. The results are obtained on a wafer implanted with 200 kV cesium ions to a dose of $10^{13}\text{Cs}^+/\text{cm}^2$. In Figure 1a, the distribution of minority carrier lifetime τ in microseconds is plotted over the wafer area, and in Figure 1b the dopant concentration N_D is plotted over the wafer area. The implantation boundary is marked by a dotted line; the implanted area is inside this line. It can be seen that the minority carrier lifetime decreases from an average value of 21 μsec measured in the unimplanted area to a value of $2.2 \times 10^{-4} \mu\text{sec}$ measured in the implanted part of the wafer. The distribution of lifetime in the implanted area is quite uniform, with the exception of a small stripe along the implantation boundary where the implantation is not uniform. The distribution of the dopant concentration N_D (Figure 1b) shows an increase of the donor concentration from $4-5 \times 10^{15}\text{cm}^{-3}$ in the unimplanted part to a maximum concentration of $1.6 \times 10^{17}\text{cm}^{-3}$ in the cesium implanted area.

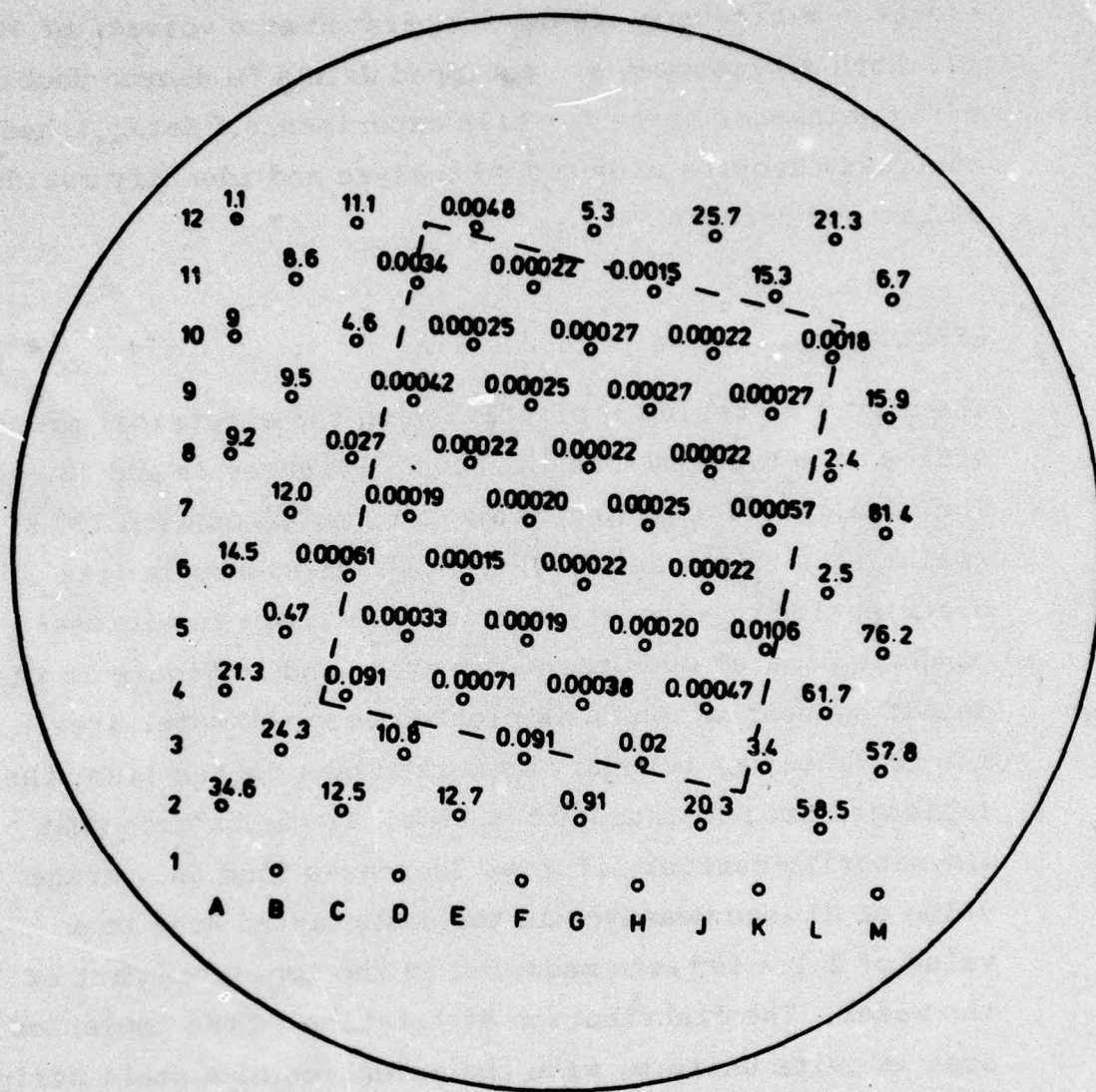


Fig. 1 a Distribution of minority carrier lifetime τ in μsec over a partially implanted silicon wafer. The cesium implanted area is within the dotted line. Implantation: $1 \times 10^{13} \text{Cs}^+/\text{cm}^2$ at 200 keV. Average values for the lifetime:

$$\tau_{\text{impl}} = 2.2 \times 10^{-4} \mu\text{sec}, \quad \tau_{\text{unimpl}} = 21 \mu\text{sec}$$

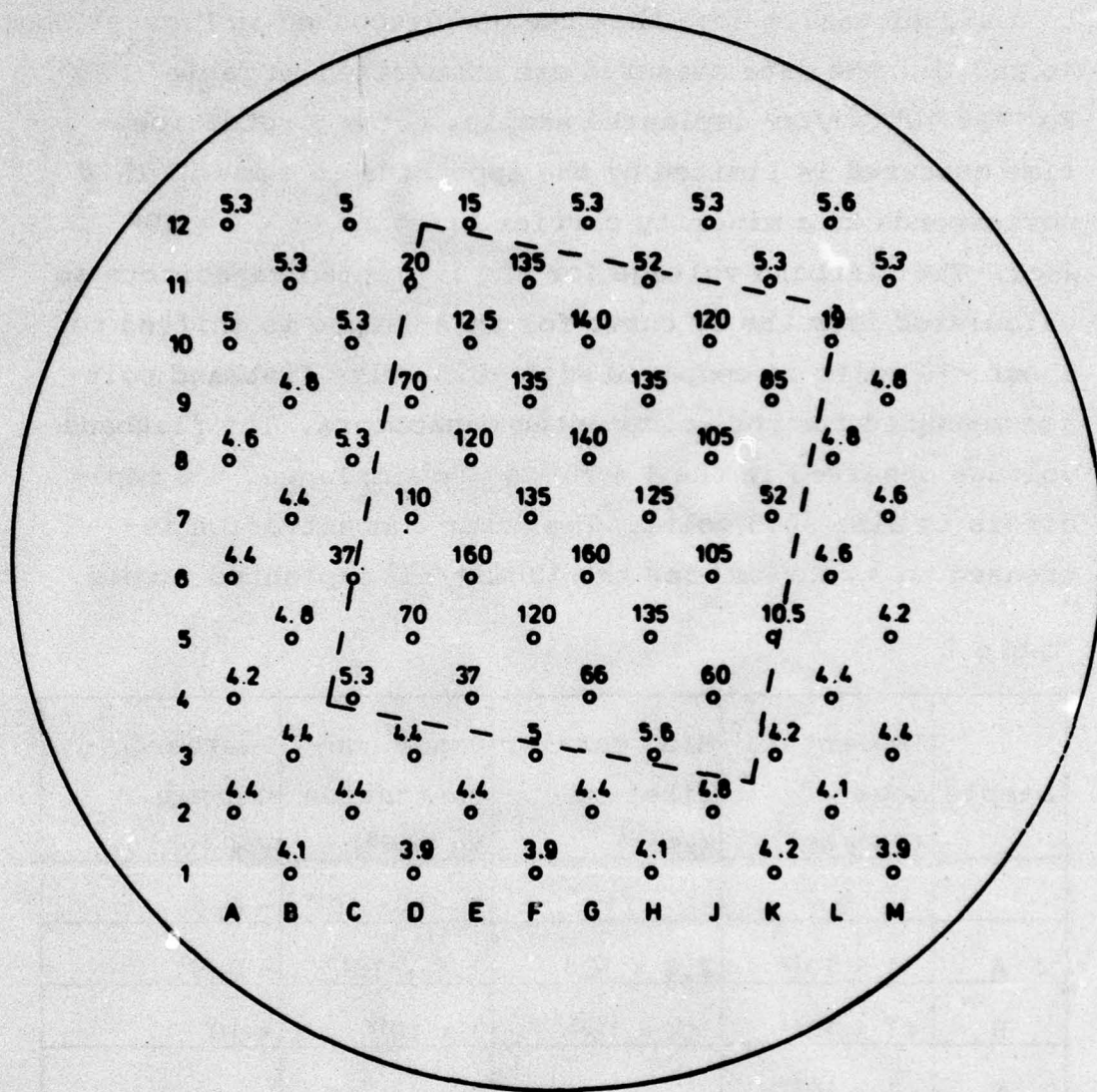


Fig. 1 b Distribution of donor doping density $N_D \times 10^{15} \text{cm}^{-3}$ over a partially implanted silicon wafer. The cesium implanted area is within the dotted line. Implantation: $1 \times 10^{13} \text{Cs}^+/\text{cm}^2$ at 200 keV. Average values for the donor doping density.

$$N_D^{\text{impl}} = 1.3 \times 10^{17} \text{cm}^{-3}$$

$$N_D^{\text{unimpl}} = 4.6 \times 10^{15} \text{cm}^{-3}.$$

Electrical measurements are also made on samples implanted to a higher cesium dose than the one discussed in Figures 1a and 1b. The data measured are summarized in Table 1. For the $10^{14}\text{Cs}^+/\text{cm}^2$ implanted sample, the MOS retention time measured is limited by the apparatus to 1 msec. This corresponds to a minority carrier lifetime of $< 4 \times 10^{-5}$ μsec . The flatband voltage for the implanted capacitors as calculated from the CV curve for this sample is shifted to about -10 volts as compared with -0.5 volts flatband voltage measured for the unimplanted capacitors. The flatband voltage observed in the $1 \times 10^{13}\text{Cs}^+/\text{cm}^2$ implanted MOS capacitors is also -0.5 volts. The donor concentration increased to $3 \times 10^{18}\text{cm}^{-3}$ for the $10^{14}\text{Cs}^+/\text{cm}^2$ implanted sample.

Table 1

Sample	Implantat. dose (Cs^+/cm^2)	Min. carrier lifetime (μsec)	Donor con- centration N_D (cm^{-3})	Flatband voltage V_{FB} (volt)
	0	21	$4 - 5 \times 10^{15}$	- 0.5
A	1×10^{13}	2.2×10^{-4}	1.6×10^{17}	- 0.5
B	1×10^{14}	$< 2 \times 10^{-5}$	3×10^{18}	- 10
C	1×10^{15}	-	-	-

For samples implanted as high as $10^{15}\text{Cs}^+/\text{cm}^2$, electrical measurements could not be evaluated. For such samples, the capacitance versus voltage curve obtained was a straight line for voltages up to the breakdown limit of about 100-150 volts.

TEM micrographs obtained from cesium implanted specimens show two different types of defects: point defect clusters and stacking faults. Point defect clusters of 10-40 Å diameter are observed in all cesium implanted samples investigated. Circular stacking faults of about 0.45 μm diameter are present in samples implanted to a dose of 10¹⁴ Cs⁺/cm² and higher. The stacking faults observed are shown in Figures 2a and 2b. As determined from bright and dark field micrographs, the faults are extrinsic in nature and surrounded by Frank partial dislocations with a/3(111) Burgers vector. This type of stacking fault is known as a circular stacking fault on (111) planes and nucleates at small strain centers in the bulk of the crystal¹¹⁾. In our case such strain centers are introduced during ion implantation. In Figures 2a and 2b the stacking faults are found to be truncated at one side. The reason for this is that during the high temperature treatment in O₂ - atmosphere both the stacking fault and the oxide thickness grow with time. After some time the Si-SiO₂ interface reaches the circular boundary of the fault area. Then further growth of the oxide cuts off more and more of the circular stacking fault. Finally it depends on the oxide thickness how much of the stacking fault is truncated. The leftover part of the stacking fault as seen in a two-beam TEM micrograph allows to reconstruct the complete circle of the fault since the angle between the (111) fault plane and the (001) surface plane is known. Thus the depth of the center of

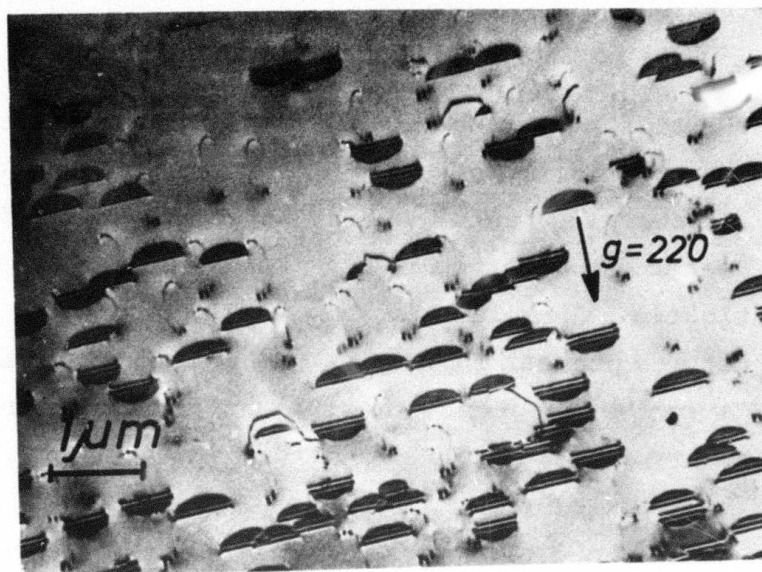


Fig. 2 a Two beam bright field transmission electron micrograph of damage induced stacking faults in silicon. Implantation: $1 \times 10^{14} \text{Cs}^+/\text{cm}^2$ at 200 keV. Nitrogen anneal and wet oxidation at 1000°C .

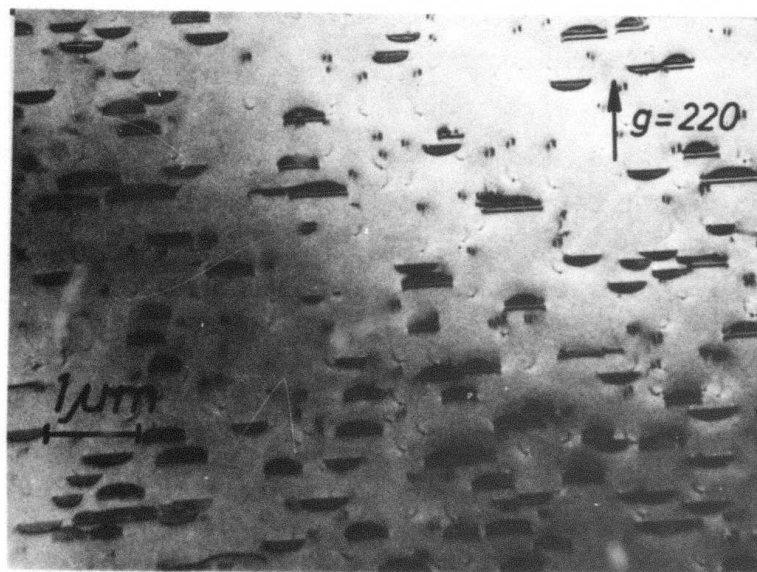


Fig. 2 b Same as Figure 2a. Implantation: $1 \times 10^{15} \text{Cs}^+/\text{cm}^2$ at 200 keV.

this circle in reference to the (001) surface of the TEM sample can be calculated. For the $10^{14}\text{Cs}^+/\text{cm}^2$ and the $10^{15}\text{Cs}^+/\text{cm}^2$ implanted samples the center of the faults are at a depth ranging from $425 \pm 300\text{\AA}$ below and $200 \pm 300\text{\AA}$ above the silicon surface, respectively. (see bars in Figure 5). The difference in the result obtained for both samples can be explained by considering the initial depth of the ion damage below the Si-surface and the different oxide thickness grown during the same heat treatment on both samples. The density of faults increases from $3.2 \times 10^8\text{cm}^{-3}$ ($10^{14}\text{Cs}^+/\text{cm}^2$) to $5 \times 10^8\text{cm}^{-3}$ ($10^{15}\text{Cs}^+/\text{cm}^2$).

The origin of the small defects is investigated by high resolution dynamic bright and dark field techniques (Figures 3a and 3b) and out of focus series micrographs (Figures 4a and 4b). In the micrographs of Figures 3a and 3b, the sample thickness t of the wedge-like crystalline foil increases from left to right. This can be seen by considering the variation of stacking fault width in the pictures (Figures 3a and 3b). These faults are the same as shown in Figures 2a and 2b but additionally are truncated at the other side by the jet-etch thinning from the back-side of the sample to the surface. In this case the sample thickness is so thin that the stacking faults intersect the top and bottom surface of the crystal. Taking $\xi_g \approx 750\text{\AA}$ for the extinction length of the (220) reflection in silicon transmitted by 100 keV electrons, we find $t \approx 1.25\xi_g$ on the left side and $t \approx 1.75\xi_g$ on the right side of Figure 3a; while $t \approx 0.25\xi_g$ on the lower left side and $t \approx 0.75\xi_g$ on the upper right side of Figure 3b.

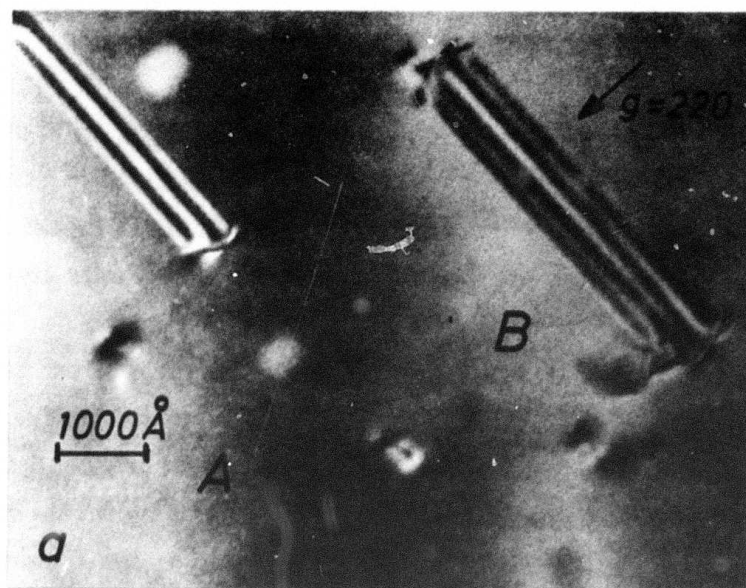


Fig. 3 a Dynamic two beam bright field electron micrograph of stacking faults, rectangular etch pits, and a high density of point defect clusters with 10-20Å size in an annealed Si sample irradiated with $10^{14}\text{Cs}^+/\text{cm}^2$. The specimen thickness t is about $1.25\xi_g$ on the left side and $1.75\xi_g$ on the right side of the dark extinction fringe.

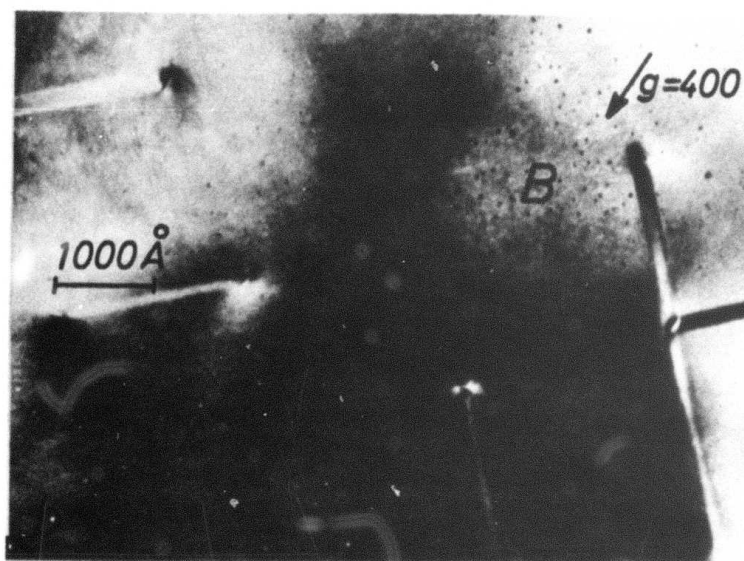


Fig. 3 b Same as Figure 3 a, showing stacking faults and point defect clusters up to 40Å in size in an annealed Si sample irradiated with $10^{15}\text{Cs}^+/\text{cm}^2$. Specimen thickness t is about $0.25\xi_g$ on the lower left side and $0.75\xi_g$ on the upper right side of the micrograph.

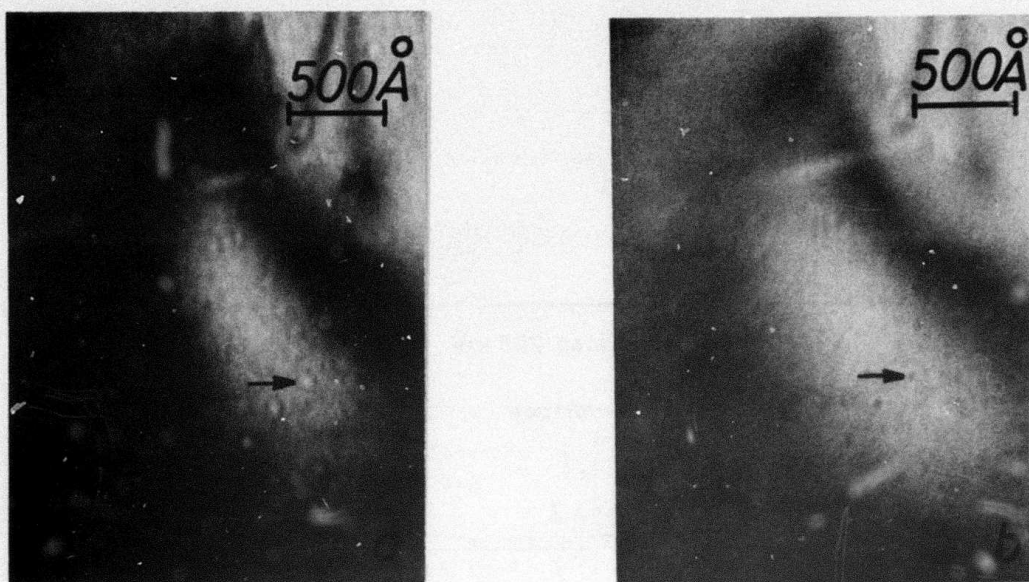


Fig. 4 Defocussed electron micrographs of point defect clusters after $10^{15}\text{Cs}^+/\text{cm}^2$ implantation after O_2 after N_2 anneal:
 a) underfocussed mode, $\zeta = -3.65 \mu\text{m}$
 b) overfocussed mode, $\zeta = +3.65 \mu\text{m}$

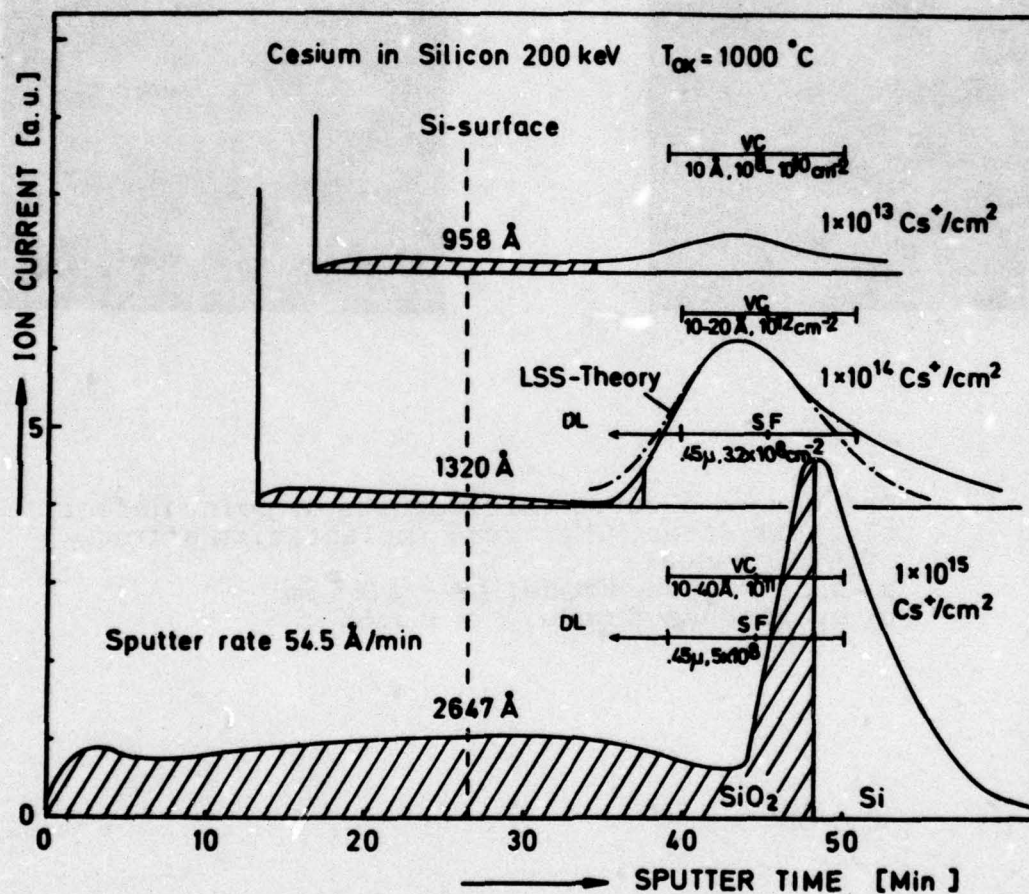


Fig. 5 Cesium profiles in SiO₂-Si double layers as measured by SIMS, for samples implanted at 200 keV with three different cesium doses. Implantation before oxidation at 1000°C.

Note that the dots visible in the micrographs show no black-white (BW) contrast because there is no strain field around them⁹⁾. The dot contrast is light on the left side of a dark fringe and dark on the right side of such a fringe. Therefore, the electron intensity within the dots is always the same just as it is found for the slightly thinner areas of the undisturbed crystal. Using structure factor contrast arguments⁹⁾ and void contrast calculations⁸⁾, it follows that the defects are a vacancy type cluster. They also can be described as vacancy rich crystal areas.

The electron micrograph of Figure 4a is taken in the underfocussed mode with a defocussed distance $\zeta = - 3.65 \mu\text{m}$, and the one in Figure 4b is taken in the overfocussed mode with $\zeta = + 3.65 \mu\text{m}$. For these two pictures the contrast in the spot center changes from light to dark. This contrast behavior again is in agreement with theoretical calculation for void-like areas of very small size^{9,10)}.

From such considerations it follows that the defects causing the small dots in the TEM micrographs are void-like structures and free of surrounding strain fields.

The results of all TEM investigations are summarized in Table 2. The size of the voids seems to increase with cesium implantation dose, whereas the dose dependence of the void density is nonlinear. Stereo micrographs show that the voids are randomly distributed throughout the depth-range found for the stacking fault nucleation centers.

Table 2

Sample	Implantat. dose (Cs ⁺ /cm ²)	Void Defects		Stacking Faults		
		Size (μ m)	Density (cm ⁻²)	Depth (\AA)	Size (\AA)	Density (cm ⁻²)
A	1×10^{13}	10	$\sim 10^8 - 10^{10}$	-	-	-
B	1×10^{14}	10-20	$\sim 10^{12}$	$+425 \pm 300$	0.45	3.2×10^8
C	1×10^{15}	10-40	$\sim 10^{11}$	-200 ± 300	0.45	5×10^8

Etch pits which are observed in sample No. B (Figure 3a) are located in the surface.

Since several authors^{12,13)} found precipitation of implanted atoms in the crystal, diffraction patterns were carefully investigated, but no extra reflection spots or rings were found. This indicates that noticeable cesium precipitation did not occur in our samples.

Cesium in-depth profiles of the SiO₂-Si double layers are shown in Figure 5. The three profiles measured are for the three different cesium implantation doses. The profiles shown in Figure 5 are drawn one above the other in such a way that the original silicon surface, which is shown as the vertical dashed line, superimposes. Starting at the original surface the oxide grows outward as well as into the silicon crystal. For equal oxidation time and temperature the oxide thickness is found to increase with im-

plantation dose. Oxide thickness as measured by ellipsometry varies between 958 and 2647 Å. Both oxide interfaces are marked by solid lines. The location of the SiO₂-Si interface during profiling is determined from a 30% increase of the stage current which is monitored simultaneously during sputtering³⁾. This increase in the stage current is caused by the increase of secondary electron emission once the underlying silicon layer is reached. From the sputter time and from the oxide thickness measured by ellipsometry, the sputter rate of silicondioxide is determined as 54.5 Å/minute.

The cesium distributions for the three different implantation doses show a peak below or at the SiO₂-Si interface. With increasing implantation dose the total cesium content in the SiO₂-Si double layer (represented by the area under the curves) increases. The cesium profiles of the 10¹³Cs⁺/cm² and of the 10¹⁴Cs⁺/cm² implanted samples show a cesium peak at a depth of about 850 Å below the original silicon surface. These peaks correspond to the original implantation peaks in the silicon. For comparison the theoretical implantation profile for 200 kV cesium implantation in silicon as calculated from the LSS theory¹⁴⁾ is included within Figure 5, and is drawn as a dashed pointed line.

For the highest implantation dose used, the cesium distribution peak is located at the SiO₂-Si interface. Due to the thicker oxide layer obtained for this dose, the peak has moved deeper into the original silicon crystal.

The cesium profiles obtained in the oxide layer are cross-lined in Figure 5. Only little cesium is found within the oxide for the $10^{13}\text{Cs}^+/\text{cm}^2$ implanted sample. For the $10^{14}\text{Cs}^+/\text{cm}^2$ implantation dose, the SiO_2 -Si interface partially overlaps the original implantation peak. For the highest implantation dose most of the cesium is within the oxide.

DISCUSSION

The results presented indicate that cesium implanted into silicon is quite effective in reducing minority carrier lifetime. A reduction of lifetime by a factor of 10^5 is achieved for an implant concentration of only $10^{13}\text{Cs}^+/\text{cm}^2$. In silicon excess minority carrier recombination is caused by chemical impurities as well as by structural defects. The cesium is introduced into the silicon through high energy (200 keV) ion implantation. As a result, considerable damage is introduced into the silicon lattice. For example, in a collision with a silicon atom a 200 keV cesium ion deposits sufficient energy to create complex defect clusters that anneal to vacancy clusters, dislocation loops and stacking faults. Within such defect clusters the single defect density is likely to be higher than the density of the chemical dopant (cesium) in the matrix. The cluster nature is important in studies of minority carrier lifetime. Trapped charges on defects inside a cluster cause a variation in the electrostatic potential, and thus can influence the recombination of minority carriers at these defects. Therefore, it is not immediately obvious

if the drastic decrease in lifetime achieved through Cs^+ implantation is caused by the defects created by the implantation and annealing procedure, or by the cesium impurity or by both. The following discussion analyzes the contribution of defect density and dopant concentration on the decrease of minority carrier lifetime obtained in silicon through 200 keV cesium ion implantation.

Nucleation and Annealing of Defects:

Before analyzing the contribution of defects observed after Cs^+ implantation in silicon and after high temperature annealing on lifetime, more details on the crystallographic structure of the defects are presented.

Three types of defects are found in Cs^+ implanted silicon: extrinsic stacking faults bounded by Frank partial dislocations, voids, and dislocation loops. An evaluation of size and density of the different defects created requires a consideration of the thermal history of the different samples investigated. The samples investigated were implanted with different Cs^+ concentrations; consequently, different amounts of lattice damage are generated. Since the oxidation rate depends on the ion damage, equal oxidation cycles lead to different oxide thicknesses for the different samples. The consequences of this effect on the TEM investigations can be seen, for example, by comparing the stacking fault images obtained for samples B and C (Figures 2a and 2b).

The stacking faults are nucleated at a depth of about 600 Å with a distribution center near to the cesium profile peak

(see bar in Figure 5). During oxidation they grow to their final size of $0.45\text{ }\mu\text{m}$ diameter. The shape of the stacking faults is completely circular until they reach the Si-SiO₂ interface. At the interface part of the fault is cut off by the growing oxide film. In the case of sample B, the stacking fault size after oxidation is larger than a semicircle. In the case of sample C, where the Si-SiO₂ interface penetrates deeper into the silicon crystal, the stacking faults are smaller in size compared to a semicircle.

Nucleation and density of stacking faults is expected to depend on the amount of damage produced through ion implantation. Stacking faults are observed in the $10^{14}\text{Cs}^+/\text{cm}^2$ and higher implanted samples, whereas, in the $10^{13}\text{Cs}^+/\text{cm}^2$ implanted sample, stacking faults are absent. The formation of stacking faults is related to the formation of a homogeneous amorphous layer produced in the silicon surface as a result of the ion implantation. The critical amorphizing dose for a 200 kV cesium implantation in silicon is not exactly known. TEM investigation of samples as implanted reveal that a dose of $5 \times 10^{13}\text{Cs}^+/\text{cm}^2$ already is sufficient to obtain a complete amorphous layer below the Si surface. Once the amorphous dose is reached or exceeded, stacking faults are nucleated within the damage region during annealing. At such high implantation doses, damage production is practically saturated. This explains the slight increase in fault density observed for samples B and C.

The second type of defect revealed by the transmission electron microscope are vacancy clusters of a size up to 40⁰Å diameter. The void-like nature of this type of defect is confirmed by two independent electron microscope experiments. To our knowledge this is the first time that voids (which are well known in metals) are observed in ion implanted and annealed silicon samples.

Usually TEM specimens are etched from the backside to the surface. Hence, a layer of perfect crystalline silicon overlays the region of residual damage after annealing. In thick areas, small point defect clusters produce only weak or no diffraction contrast. During the present investigation most of the perfect crystalline layer on top of the damaged region was oxidized and successively removed by HF. This fortunate circumstance explains why voids are easily detected in our samples. It is reasonable to expect that void density increases linearly with dose. The different thickness of the removed Si top layer in our samples is the reason for the nonlinear increase in void numbers with dose as observed in our experiments.

The density of voids increases with implantation dose in samples A and B, whereas the highest implanted sample C has a density in between. This deviation from an expected steady increase of defect density with dose is due to the fact that in the case of sample C only a small part of the voids originally present in the silicon could be seen. Stereo micrographs show that the voids are created in the highest damaged region of the silicon crystal. This layer extends from its center at or just below the cesium profile

peak 300\AA in either direction. As can be seen from Figure 5, the defect layer is completely within the silicon for samples A and B. In the case of sample C, however, most of this layer is converted by thermal oxidation into silicon-dioxide. Only the deepest part of this layer is still available for TEM investigation.

The damage induced enhanced oxidation rate also has an impact on the visibility of the third type of defect observed after cesium implantation and high temperature treatment. Transmission electron micrographs of samples with deeper implanted cesium distributions (350 kV) show dislocation loops. These loops are located underneath the silicon surface in front of the highly damaged region. They are formed during the heat treatment provided that a homogeneous amorphous silicon layer is present after implantation. In sample A the amorphizing dose is not reached, whereas in sample C the critical silicon layer is already oxidized. Only in sample B the dislocation loops are visible at the silicon surface after preferential etching of the silicon surface.

At high implantation doses (10^{14} and $10^{15}\text{Cs}^+/\text{cm}^2$) interstitial clusters are formed since the outer regions of the collision cascades overlap¹⁵⁻¹⁷). These interstitial clusters act as nucleation centers for stacking faults. The Frank partial dislocation which bounds the extrinsic stacking fault is well known to act as a sink for interstitials because of its strain field. Therefore, the stacking faults grow during the heat treatment at the expense of

the silicon interstitial supersaturation in the highly damaged region.

In the less damaged region between the silicon surface and the stacking fault nucleation centers, the silicon interstitials lead to the formation of the circular dislocation loops.

The size of the voids is somewhat dependent on implantation dose. The reasons for this are not apparent. Two possible considerations can be mentioned. The first consideration is that in spite of the presence of a sink for the interstitials, the silicon interstitials recombine partially with vacancy clusters. This would explain the small size of only 10^8 Å for the voids found in the 10^{13} Cs⁺/cm² implanted sample where stacking faults do not act as interstitial sinks. The second possibility is that for higher irradiation doses the overlap of areas occupied by defect clusters, as observed by several authors^{18,19}, becomes more probable.

Defects and Minority Carrier Lifetime:

This section discusses the impact of the defects on minority carrier lifetime. The following estimate is limited to sample A where vacancy clusters of about 10^8 Å diameter are the only defects observed after cesium implantation and successive anneal and oxidation treatment. The lifetime of holes τ_p within a reversed biased depletion region

in an n-type semiconductor is given by equation (1)²⁰:

$$(1) \quad \tau_p = \frac{2 \cosh (E_t - E_i/kT)}{v_{th} \sigma_p N_t}$$

Here $v_{th} = (3 kT/m)^{1/2}$ is the thermal velocity of the carriers. At room temperature $v_{th} \approx 10^7$ cm/sec for electrons and holes in silicon. σ_p is the capture cross-section and N_t the density of the recombination centers.

Only those centers whose energy level E_t is near the intrinsic Fermi level E_i contribute significantly to the generation rate. Minority carrier lifetime τ increases exponentially when the energy level moves away from the middle of the gap in either direction. Schulz²¹ has determined deep trap levels of ion implanted impurities in silicon by Schottky barrier capacitance voltage measurements. For implantation of alkali elements in silicon two donor levels were always observed. The upper donor level is located between 0.25 and 0.28 eV from the conduction band and is related to the radiation damage induced by the ion implantation. The lower donor level moves to a position from 0.35 to 0.5 eV from the valence band with the increasing mass of the implanted element taken from the series of group 1 in the table of elements. For cesium, the impurity related level is located at 0.5 eV from the valence band while the radiation damage level is located at 0.28 eV from the conduction band. According to Table 1 the density of voids in the $10^{15}\text{Cs}^+/\text{cm}^2$ sample is

$10^8 - 10^{10} \text{cm}^{-2}$. From this data a maximum concentration of 10^{15} voids per cm^3 within the layer thickness of about 1000\AA investigated is calculated. The capture cross-section is assumed to be of the order of the size of the voids; i.e., 10^{-14}cm^2 . With these data a minority carrier lifetime of $340 \mu\text{sec}$ is calculated for the 0.28 eV donor level. This means if this recombination center is related to the voids, a density of 10^{15}cm^{-3} has only a negligible effect on minority carrier lifetime. Such an influence is less than the impact of recombination centers which are introduced by processing and which are also present in the unimplanted part of the wafer. If we associate the vacancy clusters with the 0.5 eV level, a value of $0.07 \mu\text{sec}$ for τ is calculated for the 0.28 eV donor level. This is more than two orders of magnitude higher than the values measured. Even for this case, which is very unlikely, the density of the defects is too low to reduce the minority carrier lifetime to a level to agree with the experimental data. From such calculations it follows that the reduction of τ after low dose cesium implantation is strictly controlled (by at least 96.5%) by the properties of the cesium impurity. The vacancy clusters generated by the implantation have only a minor effect, if any at all, on lifetime.

The effect of the cesium on the lifetime of holes in silicon is comparable to the effect achieved by the addition of gold. In n-type silicon the lifetime of holes is reduced to a value of $2 \times 10^{-10} \text{ sec}$ by a gold concentration of about 10^{17}cm^{-3} ²⁰⁾. The cesium distribution can be approximated by

a rectangular profile within the implanted layer of about 600Å thickness. From this an average concentration of about $1.7 \times 10^{18} \text{Cs}^+/\text{cm}^3$ is calculated for the $10^{13} \text{Cs}^+/\text{cm}^2$ implantation dose. This would mean that about 6% of the implanted cesium is acting as recombination center in comparison to gold if the capture cross-sections for cesium and gold are similar.

Besides acting as recombination center, cesium also creates a donor center in silicon. From the high frequency CV curves a donor concentration of $1.6 \times 10^{17} \text{cm}^{-3}$ is calculated for the sample implanted with $1 \times 10^{13} \text{Cs}^+/\text{cm}^2$ ⁵⁾. For the evaluation of the doping efficiency the spatial depth of the electrical measurement has to be taken into account. The maximum width of the surface depletion layer W_{max} can be approximated by equation (2) ²¹⁾:

$$(2) \quad W_{\text{max}} = \left(\frac{4 \epsilon_{\text{si}} \epsilon_0 k T \ln(N_D/n_i)}{q N_D} \right)^{1/2}$$

Here $n_i = 1.45 \times 10^{10} \text{cm}^{-3}$ is the intrinsic carrier concentration in silicon and $\epsilon_{\text{si}} = 11.7$ the relative dielectric constant of silicon.

For a doping density of $N_D = 1.6 \times 10^{17} \text{cm}^{-3}$ a maximum depletion layer width of 825Å is calculated according to equation (2). This means that the cesium distribution is almost entirely within the depletion layer measured and contributes to the space charge capacitance. The average

cesium concentration for the $10^{13}\text{Cs}^+/\text{cm}^2$ implanted samples within this layer is $1.2 \times 10^{18}\text{cm}^{-3}$. Thus, about 13% of the cesium implanted is in an ionized state acting as donor center in silicon.

For the $10^{14}\text{Cs}^+/\text{cm}^2$ implanted sample, a donor density of $3 \times 10^{18}\text{cm}^{-3}$ is determined from CV measurements. According to equation (2) the maximum depletion layer width W_{max} is 210\AA for this donor concentration. The average cesium concentration in this layer width is about half of the maximum cesium concentration. With a doping efficiency of 12%, a donor concentration N_D of $1 \times 10^{18}\text{cm}^{-3}$ is calculated for the $10^{14}\text{Cs}^+/\text{cm}^2$ implantation. As can be seen from Figure 5, the cesium concentration increases from the silicon surface to W_{max} by a factor of four. It is known that donor centers contribute to the space charge capacitance according to their concentration multiplied by a distance factor from the silicon surface. This explains that the average donor concentration as determined from the measured CV curves ($3 \times 10^{18}\text{cm}^{-3}$) is by a factor of three higher than the value calculated from the implantation data ($1 \times 10^{18}\text{cm}^{-3}$).

The results for the doping densities after cesium implantation are in reasonable agreement with the measurements of Schulz²⁾ and of Meyer and Mayer²²⁾. Schulz obtained a doping efficiency of 10% for ion implanted cesium after an anneal in nitrogen at 700°C . From Hall measurements Meyer and Mayer determined the number of carriers to be 1-4% of the implanted cesium concentration for doses between

$4 \times 10^{13} \text{cm}^{-2}$ to $5 \times 10^{14} \text{cm}^{-2}$. This is somewhat lower than our result. From ^4He backscattering measurements they also found that less than 10% of the implanted cesium atoms lie within $0.1\text{--}0.12\text{\AA}$ of either tetrahedral interstitials or substitutional lattice locations for anneal temperatures up to 1100°C . The exact lattice site could not be specified from these measurements and the possibility of other regular sites cannot be excluded. McCaldin, et al.²³⁾, however, suggested that donor centers introduced into silicon by cesium implantation correspond to interstitial cesium ions.

For the $10^{14} \text{Cs}^+/\text{cm}^2$ implanted sample it is expected that the minority carrier lifetime is lower, by at least a factor of ten, as compared to the $10^{13} \text{Cs}^+/\text{cm}^2$ implanted sample. This means that the lifetime should be less than 10^{-11} seconds. This value is below the measurement limit of 4×10^{-11} seconds of our apparatus. Therefore, it is not possible to evaluate the effect of stacking faults on lifetime.

The SIMS measurements of Figure 5 show that in the case of sample B a small part of the cesium distribution is already within the oxide layer. This small amount of cesium at the Si-SiO₂ interface causes a shift of flatband voltage V_{FB} to -10 volts. In the case of sample C, almost half of the entire cesium at the Si-SiO₂ interface is within the oxide. Therefore, it is reasonable that flatband conditions are not reached before breakdown of the oxide. This effect made meaningful electrical measurements on this sample impossible.

SUMMARY

It is shown that the minority carrier lifetime τ in silicon can be reduced effectively by doping with cesium. A lifetime value of 2.2×10^{-10} seconds can be achieved by implantation of $10^{13}\text{Cs}^+/\text{cm}^2$ at 200 keV and subsequent anneal in nitrogen followed by an oxidation of 47 minutes at 1000°C . The reduction of τ in silicon is caused by the cesium distribution which is stable at this temperature. In comparison to gold the efficiency of the cesium recombination center is about 6%.

Some of the cesium atoms implanted are ionized; thus, acting as donor centers in silicon. For a cesium implantation dose of $10^{13}\text{Cs}^+/\text{cm}^2$ the doping efficiency is about 13%. It increases by a factor of three for an implantation dose of $10^{14}\text{Cs}^+/\text{cm}^2$. This increase, however, is probably caused by an inhomogeneous cesium distribution within the depletion layer. The results of the doping efficiency of cesium are in agreement with results obtained by Schulz (10% at 700°C) and somewhat higher than results of Meyer and Mayer (1-4%).

TEM micrographs show residual crystal defects present in the cesium implanted silicon even after anneal in nitrogen and oxidation at 1000°C . In all implanted samples vacancy clusters of 10-40Å in size are observed. To our knowledge, this is the first time that voids (which are well known in metals) are detected in annealed silicon after heavy ion implantation. The voids are created in a damaged silicon layer of 600Å thickness at the position of the damage peak

with its center near the cesium ion profile peak. The size of the voids increases from 10 to 40 Å for implantation doses ranging from 10^{13} to 10^{15} Cs⁺/cm². The density of voids also increases with cesium implantation dose. In the case of the 10^{15} Cs⁺/cm² implanted sample, part of the damaged silicon is oxidized and etched off. Therefore, the measured density is lower than for the 10^{14} Cs⁺/cm² implanted sample.

The second type of defects observed after implantation and high temperature treatment are extrinsic stacking faults bounded by Frank partial dislocations. A necessary condition for the nucleation of stacking faults is a homogeneous amorphous layer after implantation. The critical dose for the formation of an amorphous zone is about 5×10^{13} Cs⁺/cm² for a 200 keV Cesium implantation. The nucleation area for stacking faults is located within the highly damaged silicon layer where the voids are formed. The stacking faults are circular in shape and grow during anneal and oxidation to their final size of 0.45 μm diameter. The stacking fault density increases only slightly from 3.2×10^8 cm⁻² to 5×10^8 cm⁻² for implantation doses of 10^{14} and 10^{15} Cs⁺/cm², respectively. A third type of defects are dislocation loops as revealed by etch pits at the silicon surface implanted with 10^{14} Cs⁺/cm².

The effect of vacancy clusters on the lifetime of holes in silicon is calculated. Cesium implanted silicon has two energy levels in the forbidden gap. It is found that the influence of the upper donor level located at 0.28 eV on minority carrier lifetime is less than the influence of

the process introduced recombination centers. It is also found that with the 0.5 eV energy level, which is less likely to correlate with the radiation damage, the density of the voids is too low to reduce minority carrier lifetime to the values measured.

It is concluded that the decrease in lifetime achieved through Cs⁺ implantation is caused by the cesium atoms. Thus cesium presents a useful alternative for device applications which require gold as a dopant.

ACKNOWLEDGMENTS

The authors wish to thank C. Schneider for the sample preparation, H. Ilker for help with the SIMS- and TEM-investigations, and E. Gorey for the ellipsometer measurements.

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